AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in this application.

Listing of Claims:

1. (Currently Amended) A method for storing and reading data in a write-once memory array, the method comprising:

(a) inverting a plurality of bits representing data to be stored in a write-once memory array irrespective of a number of logic one bits in the plurality of bits;

(b) storing the inverted plurality of bits in the write-once memory array;

(c) reading the inverted plurality of bits from the write-once memory array; and

(d) inverting the inverted plurality of bits read from the write-once memory array.

2. (Currently Amended) The ~~invention~~ method of Claim 1, wherein act (a) is performed by a data storage device coupled with a memory device comprising the write-once memory array.

3. (Currently Amended) The ~~invention~~ method of Claim 2, wherein the data storage device comprises a device selected from the group consisting of a digital audio player, a digital audio book, an electronic book, a digital camera, a game player, a general-purpose computer, a personal digital assistant, a portable telephone, a printer, and a projector.

4. (Currently Amended) The ~~invention~~ method of Claim 1, wherein act (a) is performed by a controller of a memory device comprising the write-once memory array.

5. (Currently Amended) The ~~invention~~ method of Claim 1, wherein act (d) is performed by a data reading device coupled with a memory device comprising the write-once memory array.

6. (Currently Amended) The ~~invention~~ method of Claim 5, wherein the data reading device comprises a device selected from the group consisting of a digital audio player, a digital audio book, an electronic book, a digital camera, a game player, a general-purpose computer, a personal digital assistant, a portable telephone, a printer, and a projector.

7. (Currently Amended) The ~~invention~~ method of Claim 1, wherein act (d) is performed by a controller of a memory device comprising the write-once memory array.

8. (Currently Amended) A memory device comprising:

a write-once memory array storing a plurality of bits representing data; and

a controller coupled with the write-once memory array and operative to invert the plurality of bits representing the data irrespective of a number of logic one bits in the plurality of bits when the plurality of bits is read from the write-once memory array.

9. (Currently Amended) The ~~invention~~ memory device of Claim 8, wherein the controller is further operative to invert a plurality of bits representing data to be stored in the write-once memory array.

10. (Currently Amended) The ~~invention~~ memory device of Claim 8, wherein the memory device comprises a solid-state memory device.

11. (Currently Amended) The ~~invention~~ memory device of Claim 8, wherein the memory device comprises an optical memory device.

12. (Currently Amended) A method for redefining an initial, un-programmed digital state of a write-once memory array, the method comprising:

(a) providing a write-once memory array comprising a plurality of write-once memory cells, the plurality of write-once memory cells comprising an initial, un-programmed digital state that can be switched to an alternative, programmed digital state; and

(b) redefining the initial, un-programmed digital state of the plurality of write-once memory cells as the alternative, programmed digital state by storing bits in the plurality of write-once memory cells in an inverted form irrespective of a number of logic one bits in the plurality of bits.

13. (Currently Amended) The ~~invention~~ method of Claim 12, wherein the initial, un-programmed digital state comprises Logic 1, and wherein the alternative, programmed digital state comprises Logic 0.

14. (Currently Amended) The ~~invention~~ method of Claim 12, wherein the initial, un-programmed digital state comprises Logic 0, and wherein the alternative, programmed digital state comprises Logic 1.

15. (Currently Amended) The ~~invention~~ method of Claim 1~~, 8,~~ or 12, wherein the write-once memory array comprises a three-dimensional memory array.

16. (Currently Amended) The ~~invention~~ method of Claim 1~~, 8,~~ or 12, wherein the write-once memory array comprises a two-dimensional memory array.

17. (New) The memory device of Claim 8, wherein the write-once memory array comprises a three-dimensional memory array.

18. (New) The memory device of Claim 8, wherein the write-once memory array comprises a two-dimensional memory array.

19. (New) The method of Claim 1, wherein the plurality of bits are inverted even when a number of logic one bits in the plurality of bits does not exceed fifty percent of a total number of bits in the plurality of bits.

20. (New) The memory device of Claim 8, wherein the plurality of bits are inverted even when a number of logic one bits in the plurality of bits does not exceed fifty percent of a total number of bits in the plurality of bits.

21. (New) The method of Claim 12, wherein the controller is operative to invert the plurality of bits even when a number of logic one bits in the plurality of bits does not exceed fifty percent of a total number of bits in the plurality of bits.